REMARKS

Entry of the above amendment and reconsideration of the above-referenced application in view of the above amendment, and of the following remarks, is respectfully requested.

Claims 1-8 and 17-18 are pending in this case. Claim 1 is amended herein and claims 17 and 18 are added herein.

The Examiner rejected claims 1, 2, 6 and 7 under 35 U.S.C. § 102(e) as being anticipated by Saia et al. (U.S. Pat. No. 5,874,770).

Applicant respectfully submits that claim 1 is unanticipated by Saia et al as there is no disclosure or suggestion in Saia of a thin film resistor embedded within a multi-level dielectric layer between and physically separated in a vertical direction from a lower metal interconnect layer and an upper metal interconnect layer. Saia teaches a resistor that extends along the edges of a dielectric 10, rather than being embedded within it as required by the claim. In addition, the resistor material 16,18 is in direct physical contact with the metal interconnect levels rather than being physically separated in a vertical direction from the upper and lower metal interconnect layers. Accordingly, Applicant respectfully submits that claim 1 and the claims dependent thereon are unanticipated by Saia et al.

The Examiner rejected claim 3 under 35 U.S.C. §103(a) as being unpatentable over Saia et al. (U.S. Pat. No. 5,874,770).

Applicant respectfully submits that claim 3 is patentable over Saia et al for the same reasons discussed above relative to claim 1 from which claim 3 depends.

The Examiner rejected claims 4, 5 and 8 under 35 U.S.C. §103(a) as being unpatentable over Saia et al. as applied to claim 1, and further in view of Linn et al. (U.S. Patent No. 5,547,896).

Applicant respectfully submits that claims 4, 5, and 8 are patentable over Saia et al in view of Linn et al for the same reasons discussed above r lative to claim 1 from which these claims depend. Linn et al is applies to teach an

electrode overlaid by a TiW or TiN hardmask and th interchangeability between SiCr and NiCr. The references as combined fail to teach a thin film resistor embedded within a multi-level dielectric layer between and physically separated in a vertical direction from a lower metal interconnect layer and an upper metal interconnect layer.

New claims 17 and 18 are added to more completely cover that which Applicant regards as the invention. Independent claim 17 requires an integrated circuit that comprises a semiconductor chip that itself comprises the claimed thin film resistor. This is in contrast to the teachings of Saia in which the resistor is located external to the circuit chip 44.

Attached hereto is a marked up version of the changes made to the specification and claims by the current amendment. The attached page is captioned "**Version with Markings to Show Changes Made**."

In light of the above, Applicant respectfully requests withdrawal of the Examiner's rejections and allowance of claims 1-8 and 17-18. If the Examiner has any questions or other correspondence regarding this application, Applicant requests that the Examiner contact Applicant's attorney at the below listed telephone number and address.

Respectfully submitted,

Texas Instruments Incorporated
P.O. Box 655474, M/S 3999
Dallas, TX 75265
PHONE: 214-532-9348
FAX: 972 917-4418

Jacqueline J. Garner
Reg. No. 36,144

Version with Markings to Show Changes Mad

Claim 1 is proposed to be amended as follows:

1. (amended) An integrated circuit comprising:

a lower metal interconnect layer located over a semiconductor body;

a multi-level dielectric layer located over said lower interconnect layer;

an upper metal interconnect layer located over said multi-level dielectric layer; and

a thin film resistor [located] embedded within said multi-level dielectric layer between and physically separated in a vertical direction from said lower metal interconnect layer and said upper metal interconnect layer.

Claims 17 and 18 are added herein.